TBA 810S
TBA 810AS

7 W AUDIO POWER AMPLIFIER WITH THERMAL SHUT-DOWN

The TBA810 S is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier.

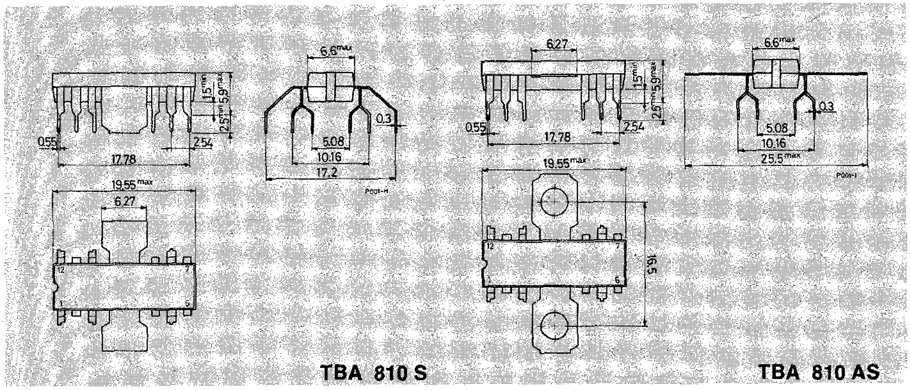
The TBA810 S provides 7 W output power at 16 V/4 Ω, 6 W at 14.4 V/4 Ω, 2.5 W at 9 V/4 Ω, 1 W at 6 V/4 Ω and works with a wide range of supply voltages (4 to 20 V); it gives high output current (up to 2.5 A), high efficiency (75% at 6 W output), very low harmonic and cross-over distortion. The circuit is provided with a thermal limiting circuit which fundamentally changes the criteria normally used in determining the size of the heatsink, in addition the TBA 810 S/AS can withstand short-circuit on the load for supply voltages up to 15 V.

The TBA 810AS has the same electrical characteristics as the TBA 81OS, but its cooling tabs are flat and pierced so that an external heatsink can easily be attached.

	V_s	Supply voltage	20	V
	I_o	Output peak current (non-repetitive)	3.5	A
→	I_o	Output peak current (repetitive)	2.5	A
→	P_{tot}	Power dissipation: at $T_{amb} \leq$ 80 °C (for **TBA 810 S)**	1	W
		at $T_{tab} \leq$ 100 °C (for **TBA 810 AS)**	5	W
	T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

MECHANICAL DATA

Dimensions in mm



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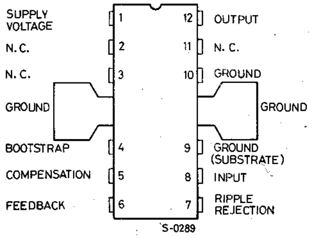
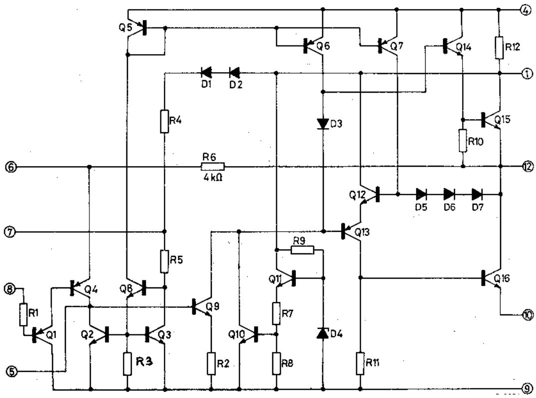
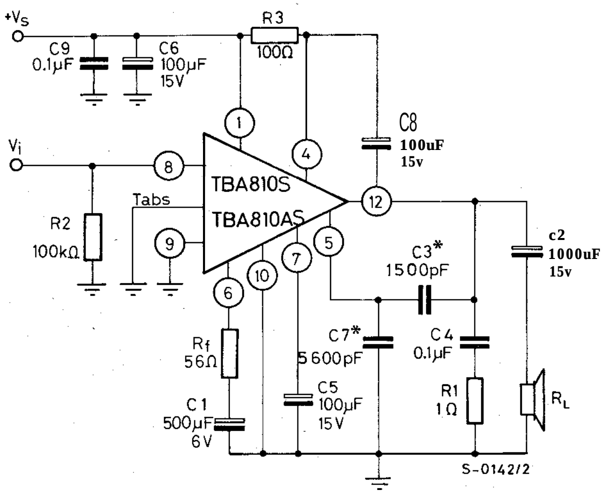
CONNECTION AND SCHEMATIC DIAGRAM





TEST AND APPLICATION CIRCUIT



* C3, C7 see fig. 6

THERMAL DATA

			TBA 810S	TBA 81 OAS
$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12 °C/W	10 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70* °C/W	80 C/W

* Obtained with tabs soldered to printed circuit with minimized copper area

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; T_{amb} = 25 °C)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 12)	V_s = 14.4 V	6.4	7.2	8	V
I_d	Quiescent drain current			12	20	mA
I_b	Bias current (pin 8)			0.4	4	μA
P_o	Output power	d = 10% R_L = 4 Ω f = 1 kHz				
		V_s = 16 V		7		W
		V_s = 14.4 V	4.6	6		W
		V_s = 9 V		2.5		W
		V_s = 6 V		1		W
$V_{i(rms)}$	Input saturation voltage				220	mV
V_i	Input sensitivity	P_o = 6 W V_s = 14.4 V R_L = 4 Ω f = 1 kHz				
		R_f = 56 Ω		80		mV
		R_f = 22 Ω		35		mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (-3 dB)	Vs = 14.4 V RL=4Ohm				
		C3 = 820 pF		40 to 20,000		Hz
		C3= 1500pF		40 to 10,000		Hz

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
d	Distortion	Po = 50 mW to 3 W Vs = 14.4 v RL = 4 Ω f = 1 kHz		0.3		%
Gv	Voltage gain (open loop)	Vs = 14.4 v RL= 4 Ω f = 1 kHz		80		dB
Gv	Voltage gain (closed loop)	Vs = 14.4 v RL= 4 Ω f = 1 kHz	34	37	40	dB
eN	Input noise voltage	Vs = 14.4 v Rg = 0 B (-3 dB) = 20 Hz to 20,000 Hz		2		µV
i_N	input noise current	Vs = 14.4 v B (-3 dB) = 20 Hz to 20,000 Hz		0.1		nA
	Efficiency	Po=5W Vs = 14.4 v RL=4Ohm f = 1 kHz		70		%
→ SVR	Supply voltage rejection	Vs = 14.4 V RL= 4 Ω frippre = 100 Hz		48		dB
→ Id	Drain current	Po=6W Vs = 14.4 v RL= 4 Ω		600		mA
→	* Thermal shut-down case temperature	Ptot = 2.8 w		120		°C

*See figs. 7 and 16

Fig. 1 - Typical output power versus supply voltage

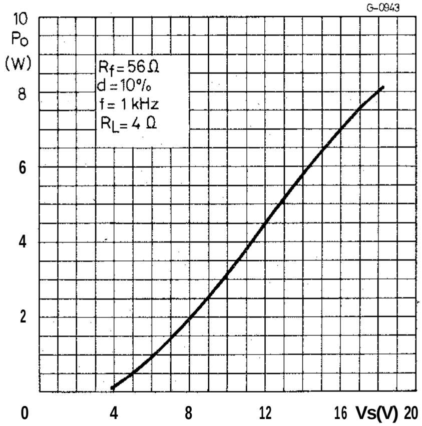


Fig. 2 - Maximum **power dissipation versus supply** voltage (sine wave operation)

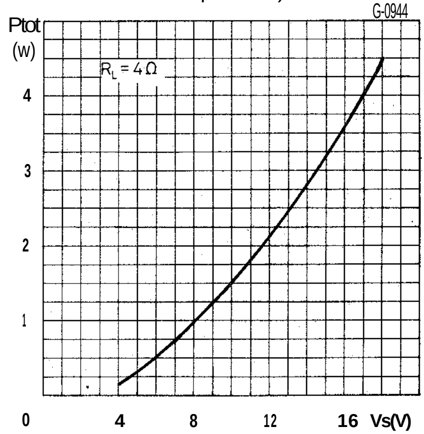


Fig.3 - Typical distortion versus output power

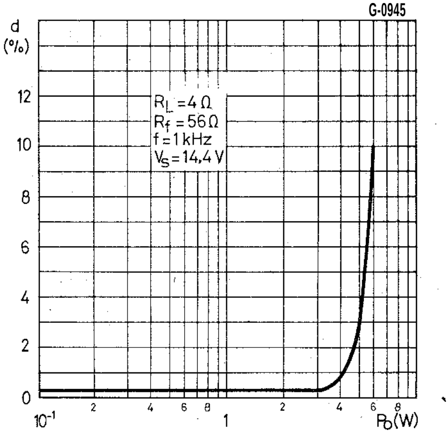


Fig. 4 - Typical distortion **versus frequency**

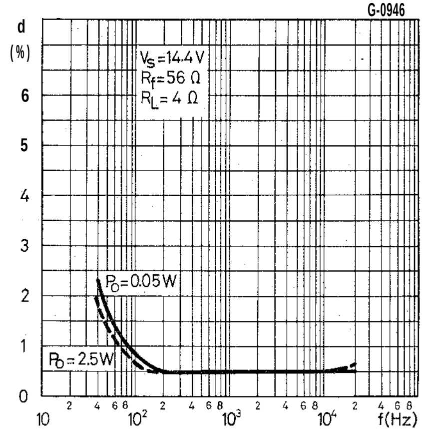


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Fig. 5 - Typical relative voltage gain (closed loop) and typical input **voltage** versus feedback resistance (Rf)

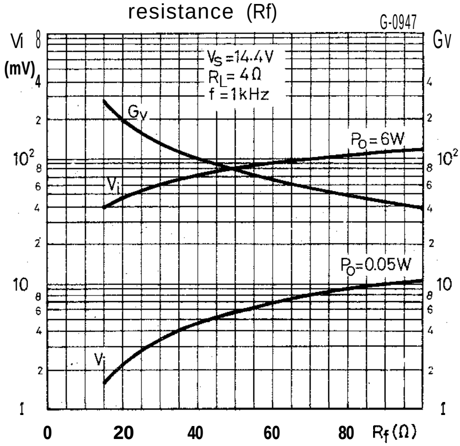


Fig. 6 -Typical value of C3 versus Rf for various values of B

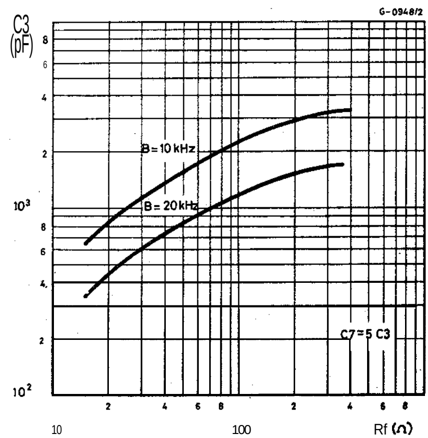


Fig. 7 - Typical power dissipation and efficiency **versus output power**

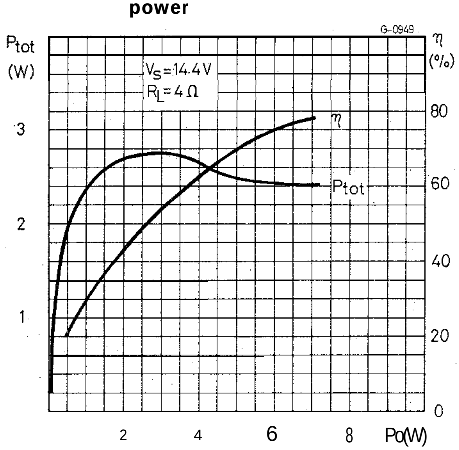


Fig. 8 - Typical quiescent output voltage (pin 12) versus supply voltage

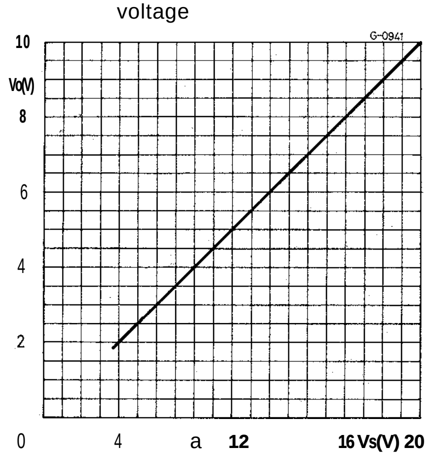


Fig. 9 - Typical quiescent current versus supply voltage

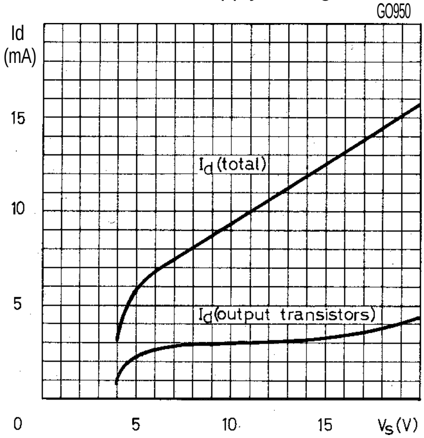
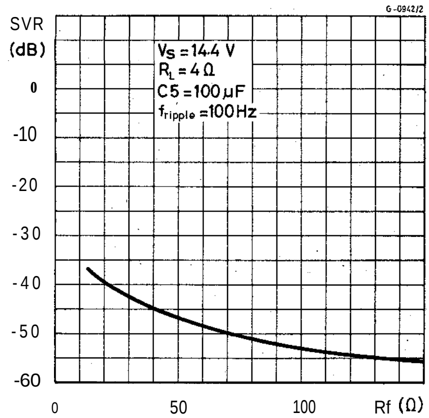
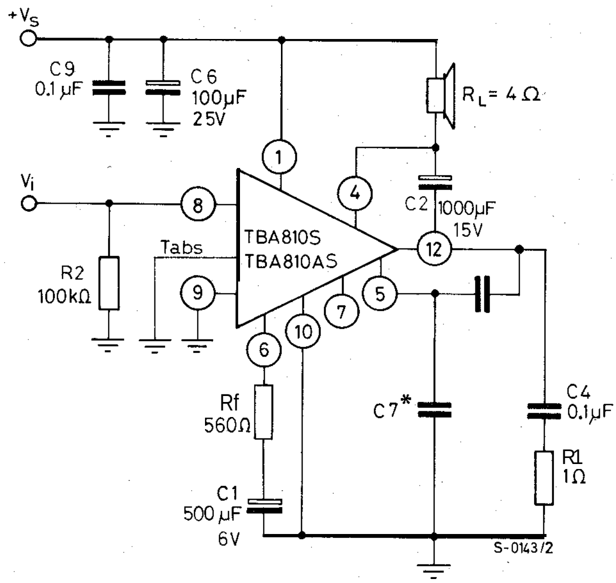


Fig. 10 - Typical supply voltage rejection



For portable equipment the circuit in Fig. 11 has the advantages of fewer external components and a better behaviour at low supply voltages (down to 4 V).

Fig. 11 - Typical circuit with load connected to the supply voltage



* C3, C7 see fig. 6

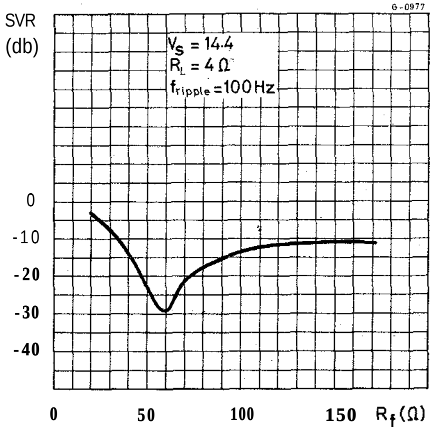


Fig. 12 - Typical supply voltage rejection versus Rf (fig. 11 circuit)

MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heat sink (TBA 810 AS - fig. 13) or by soldering them to an area of copper on the printed circuit board (TBA 810s - fig. 14).
During soldering the tabs temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.
Fig. 15a and 15b show two ways that can be used for mounting the device.

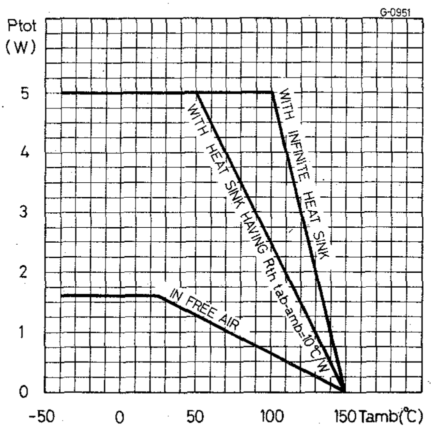


Fig. 13 - Maximum power dissipation versus ambient temperature (for TBA 810 AS only)

Fig. 14 - Maximum power dissipation versus copper area ,of the P.C. board (for TBA 810s only)

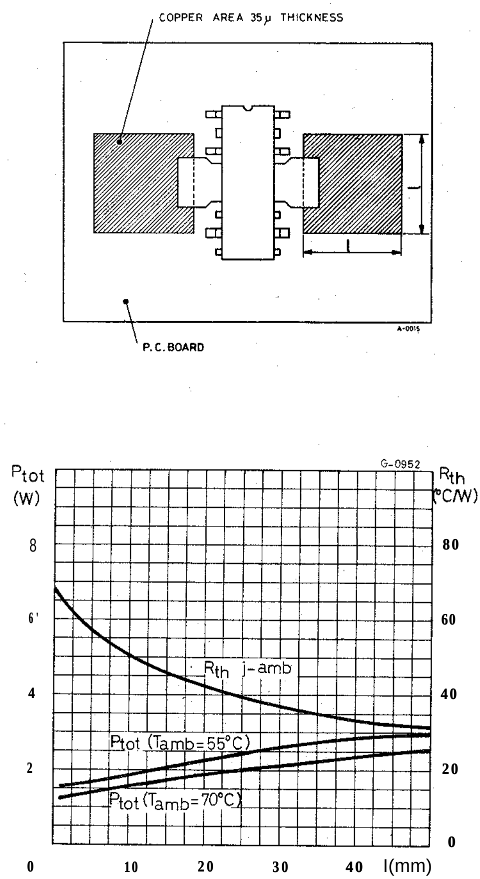


Fig. 15a shows a method, of mounting the TBA 810S that is satisfactory both from the point of view of heat dissipation and from mechanical considerations. For TBA 810AS the desired thermal resistance is obtained by fixing the elements shown in fig. 15b, to a suitably dimensioned plate. This plate can also act as a support for the whole printed circuit board; the mechanical stresses do not damage the integrated circuit. This is firmly fixed to the element, in fig. 15b.

Fig. 15a

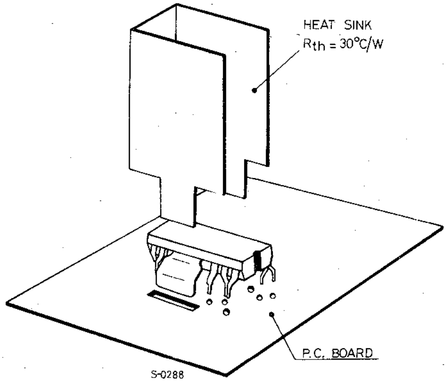
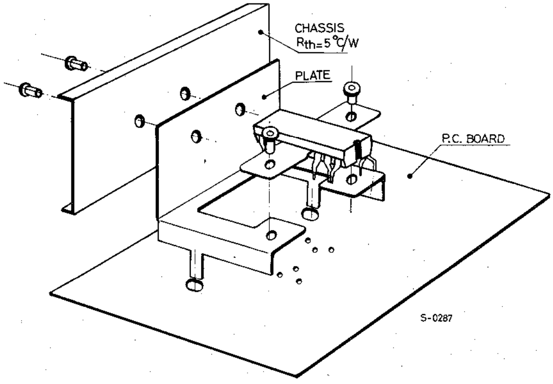


Fig. 15b



THERMAL SHUT-DOWN

The presence of a therms! limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily supported

2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of too high a junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced (fig. 16).

Fig. 16 - Output power and drain current versus package temperature

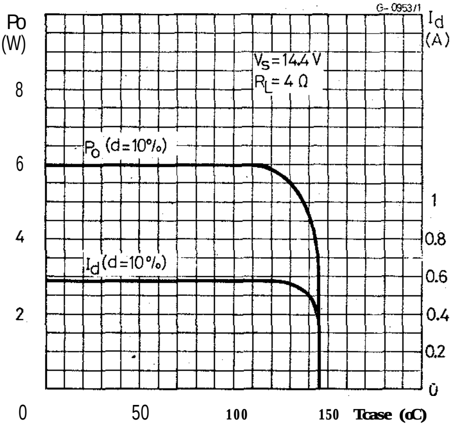


Fig. 17 - P.C. board and component layout for the test and application circuit

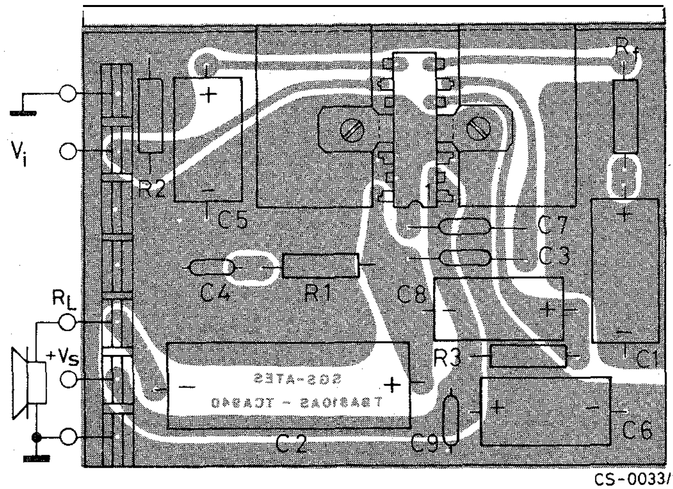


Fig. 18 - P.C. board and component layout for the fig. 11 circuit